IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): ITO et al.	Atty. Dkt.: 01-149-DIV
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME	

Commissioner for Patents
Arlington, VA 22202

Date: February 26, 2004

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are being submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,

David G. Posz
Reg. No. 37,701

Posz & Bethards, PLC
11250 Roger Bacon Drive, Suite 10
Reston, VA 20190
(703)707-9110 (phone)
Customer No. 23400

FORM PTO-1449	ATTY. DKT NO. 01-149-DIV	SER. NO.
	APPLICANT **ITO et al.**	
	FILING DATE February 26, 2004	GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		5,448,083	09-1995	Kitagawa et al.		
		6,110,799	08-2000	Huang	438	430
		5,895,951	04-1999	So et al.	257	330
		6,213,869	04-2001	Yu et al.	458	236
		5,998,836	12-1999	Williams		
		5,072,266	12-1991	Bulucea et al.		
		6,049,108	04-2000	Williams		
		6,140,678	10-2000	Grabowski et al.		
		5,907,776	05-1999	Hshieh et al.	438	270

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	YES	TRANSLATION NO	
										Eng. Abstract
		JP-A-5-206264	8/13/94	JAPAN						X
		JP-A-5-226351	9/3/93	JAPAN						X
		JP-A-6-151867	5/31/94	JAPAN						X
		JP-A-7-249770	9/26/95	JAPAN						X
		JP-A-8-264772	10/11/96	JAPAN						X
		JP-B2-2590863	Published on 9/19/88	JAPAN						X

* Full English text of the JP Document will be available in machine-translated form from JP (Japanese Patent Office) English language web site at **http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX**.

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

		S. Wolf, "Silicon Processing for the VLSI Era," Volume 2 – "Process Integration," Lattice Press (Sunset Beach, CA), ISBN 0-961672-4-5 (1990); particularly pages 658-663.

EXAMINER	DATE CONSIDERED

Rev. 10/94 (Form 3.05)